TEXAS INSTRUMENTS

TPS54610EVM

6-Amp Externally Compensated SWIFT™ Regulator Evaluation Module

User's Guide

August 2001

PMP PD & PS

SLVU054

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the TPS54610 6-amp externally compensated SWIFT™ regulator evaluation module (EVM). The user's guide includes a schematic diagram and bill of materials.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

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Chapter 1

Introduction

This chapter contains background information for the TPS54610 and support documentation for the TPS54610 evaluation module. The EVM performance specifications are also given.

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1.1 Background

The TPS54610 evaluation module (EVM) uses the TPS54610 synchronous buck regulator to provide a 3.3-V output over an input range of 4.0 V to 6.0 V and over a load range of 0 A to 6 A. The EVM is designed to be easily modified. Additional pads support multiple input and output capacitors, and the inductor pads are large to accommodate different inductors. A jumper is provided to allow the switching frequency to be easily changed from 350 kHz to 550 kHz.

The MOSFETs of the TPS54610 are incorporated inside the TPS54610 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs gives the TPS54610 high efficiency and helps to keep the junction temperature low at high output currents. The compensation components, external to the IC, allow for an adjustable output voltage and a customizable loop response.

1.2 Performance Specification Summary

Table 1–1 provides a summary of the TPS54610 EVM performance specifications. All specifications are given for an ambient temperature of 25°C, unless otherwise noted.

Table 1–1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		4	5	6	V
Output voltage set point			3.3		V
Output current range	V_{IN} = 5 V	0		6	A
Line regulation	I_O = 6 A	–5		+5	mV
Load regulation	V_{IN} = 5 V	–5		+5	mV
Load transient response	I_O = 1 A to 5 A, $t_{(rise)}$ = 10 µs		–50		mV_{PK}
			100		µs
	I_O = 5 A to 1 A, $t_{(fall)}$ = 10 µs		50		mV_{PK}
			150		µs
Loop bandwidth	V_{IN} = 5 V, I_O = 6 A		25		kHz
Phase margin	V_{IN} = 5 V, I_O = 6 A		75		°
Input ripple voltage				250	mV_{PP}
Output ripple voltage				18	mV_{PP}
Output rise time		4.7	8.4	15	ms
Operating frequency	V_{SYNCH} = 0 V	280	350	420	kHz
	V_{SYNCH} = V_{IN}	440	550	660	
Efficiency	V_{IN} = 5 V, I_O = 1.5 A		94%		

1.3 Modifications

The TPS54610 EVM is designed to support numerous types of input capacitors, output capacitors, and inductors (see Top-Side Layout Figure 3–1, and EVM schematic Figure 4–1). C3 provides pads for a surface mount input capacitor, while the holes of C1 can be used for through-hole input capacitors. Similarly, C10 and C11 provide pads for surface-mount output capacitors, while the holes of C12 can be used for through-hole output capacitors. The pads of L1, which are intentionally large, can accommodate a variety of power inductors. When changing the output filter, the compensation values must also be changed to ensure stability. The SWIFT™ Designer software tool or Texas Instruments Application Note *SLVA104 – Designing With Externally Compensated SWIFT™ Regulators* can be used to assist in the calculation of compensation components. Both SWIFT™ Designer software and application note SLVA104 are available for download at the Texas Instruments web site.

The TPS54610 EVM can be easily configured to switch at either 350 kHz or 550 kHz by changing the location of jumper JP1. Alternatively, by using RT (R3), the switching frequency can be trimmed to any value between 280 kHz and 700 kHz. A plot of the value of RT versus the switching frequency is given in Figure 1–1.

The output voltage of the TPS54610 EVM can be adjusted to any value down to 0.9 V by changing only one component value (R2). The value of R2 for a specific output voltage can be calculated by using Equation 1–1. Table 1–2 lists the value of R2 for some common bus voltages.

Equation 1–1.

$$R_2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V}$$

Changing the value of C2 can modify the slow start time of the TPS54610 EVM. Use Equation 1–2 to calculate the value of C2 for a specific slow start time. With C2 left open, the slow start time is typically 3.6 ms. The slow start time can not be made faster than 3.6 ms.

Equation 1–2.

$$C_2 = \frac{T_{SS} \times 5\ \mu A}{0.891\ V}$$

Figure 1–1. Frequency Trimming Resistor Selection Graph

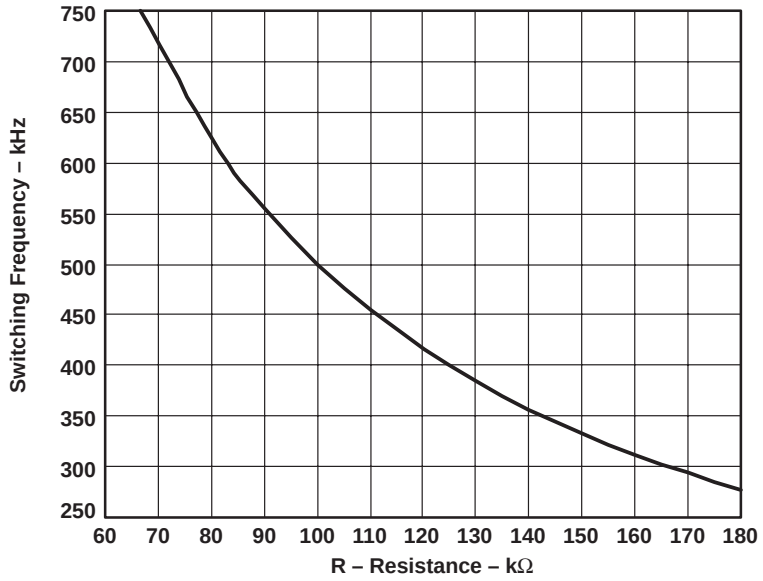

Table 1–2. Output Voltage Programming

Output Voltage (V)	R2 (kΩ)
0.9	1000
1.2	28.7
1.5	14.7
1.8	9.76
2.5	5.49
3.3	3.74

Chapter 2

Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54610 EVM. It also presents the test results and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

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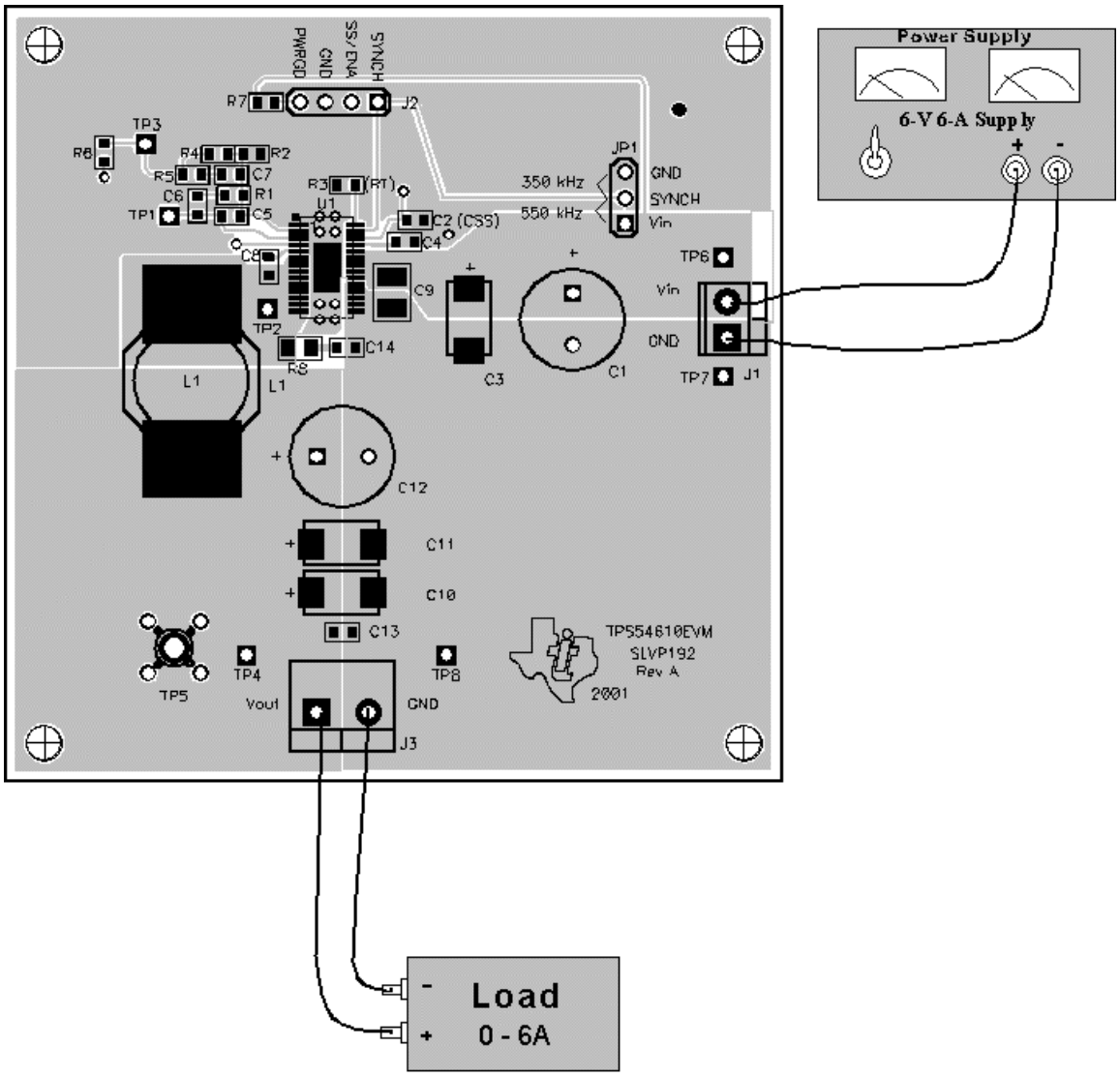
2.1 Input/Output Connections

The TPS54610 EVM has the following input/output connections: J1 (V_{in} and GND) and J3 (V_{out} and GND). A diagram showing the connection points is shown in Figure 2–1. Connect a power supply capable of supplying 6 A to J1 through a pair of 20 AWG wires. Connect the load to J3 through a pair of 16 AWG wires. Minimize wire lengths to reduce losses in the wires. Test point TP5 provides easy connection for an oscilloscope voltage probe to monitor the output voltage.

Figure 2–1. Connection Diagram



2.2 Loop Characterization Setup

The TPS54610 EVM contains a 49.9-Ω resistor (R6) in the feedback path for use in measuring the loop response. Test points on either side of R6 (TP4 and TP3) provide connection points for network analyzer signals. By injecting a small AC signal across R6, the loop gain and phase can be measured from one side of R6 to the other. Because the value of R6 is small in relation to the value of R4, it does not affect the output voltage set point of the regulator.

2.3 Efficiency

The TPS54610 EVM efficiency peaks at around 1.5 A of load current. At full load this drops to around 89%. Figure 2–2 shows the typical efficiency for a 5-V input and an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly higher at 350 kHz than at 550 kHz due to the gate and switching losses in the MOSFETs. The total board losses are shown in Figure 2–3.

Figure 2–2. Measured Efficiency

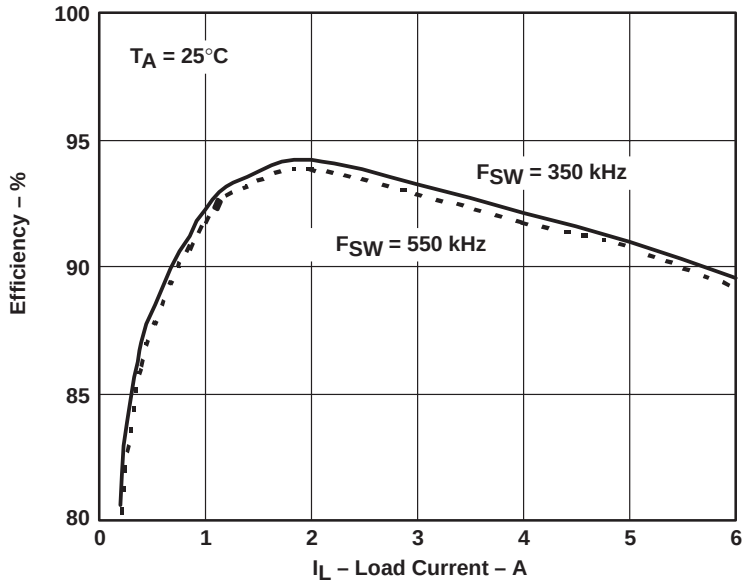
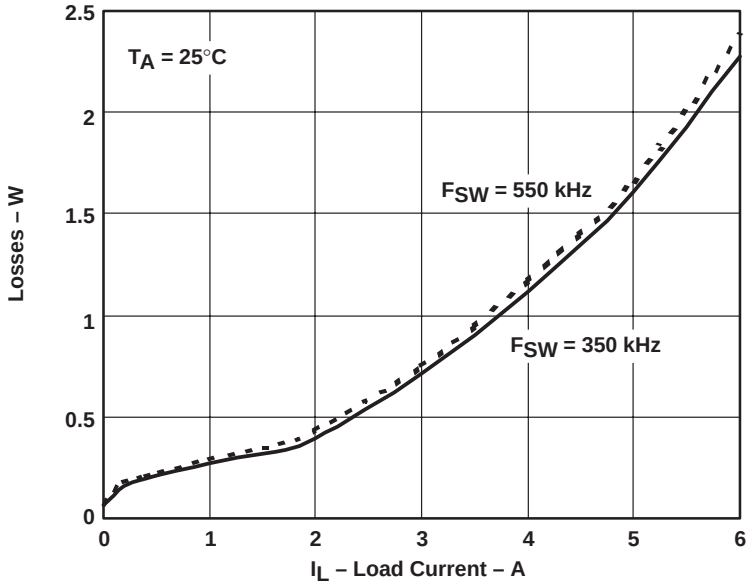


Figure 2–3. Measured Board Losses



2.4 Thermal Performance

The junction temperature is plotted versus the load current with a 5-V input voltage and a 25°C ambient temperature in Figure 2–4. The case temperature is plotted in Figure 2–5. The low junction-to-case thermal resistance of the PWP package, along with a good board layout, helps to keep the junction temperature low at high output currents. With a 5-V input source and a 6-A load, the junction temperature is approximately 60°C, while the case temperature is approximately 55°C.

Figure 2–4. Measured Junction Temperature at 25°C Ambient

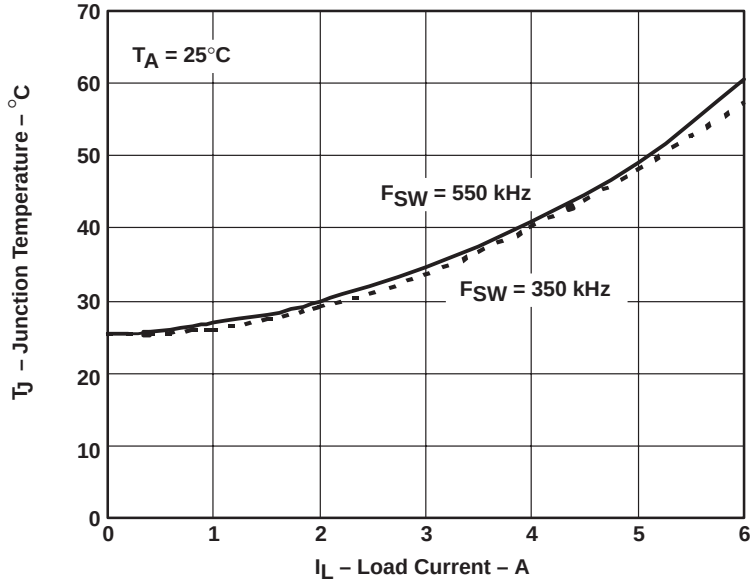
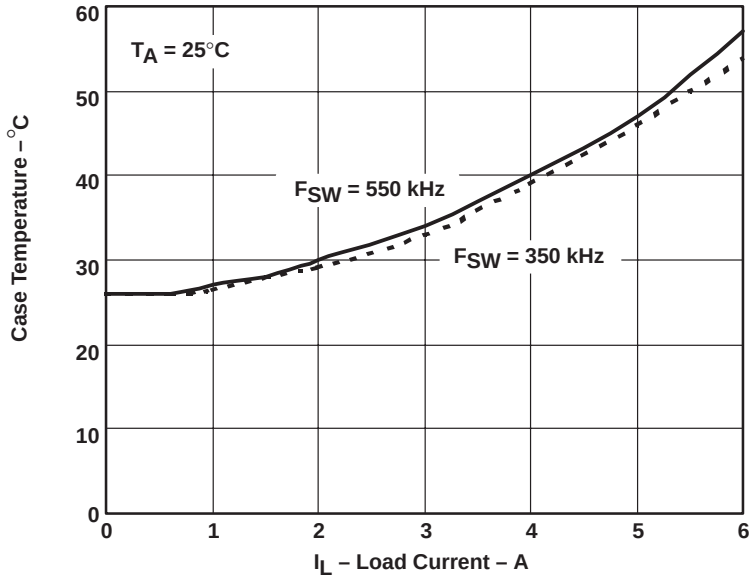


Figure 2–5. Measured Case Temperature at 25°C Ambient



2.5 Output Voltage Regulation

The output voltage load regulation with a 5-V input and a 25°C ambient temperature is shown in Figure 2–6. The output voltage line regulation is shown in Figure 2–7. Over the input voltage range of 4.0 V to 6.0 and the load range of 0 A to 6 A, the output voltage varies less than 0.3%.

Figure 2–6. Measured Load Regulation

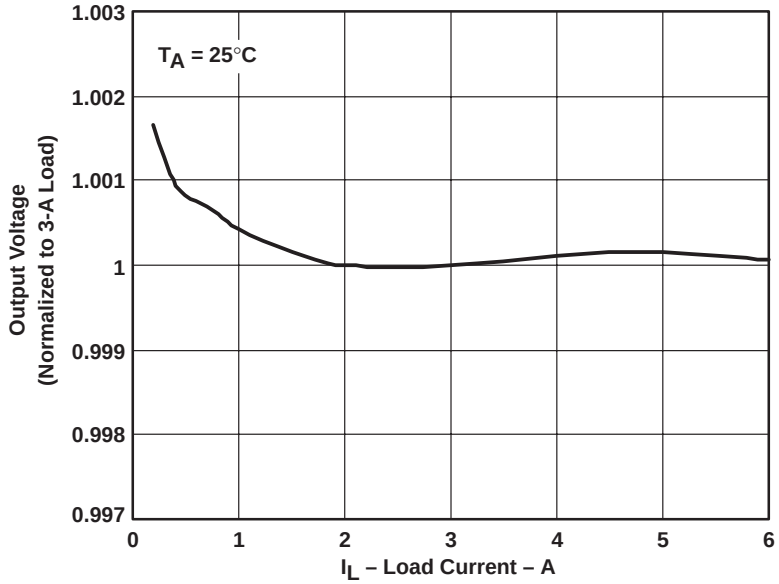
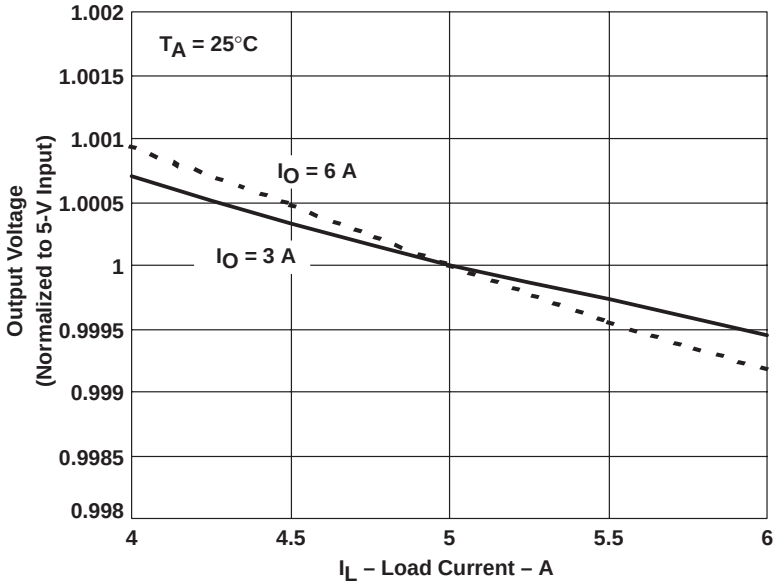


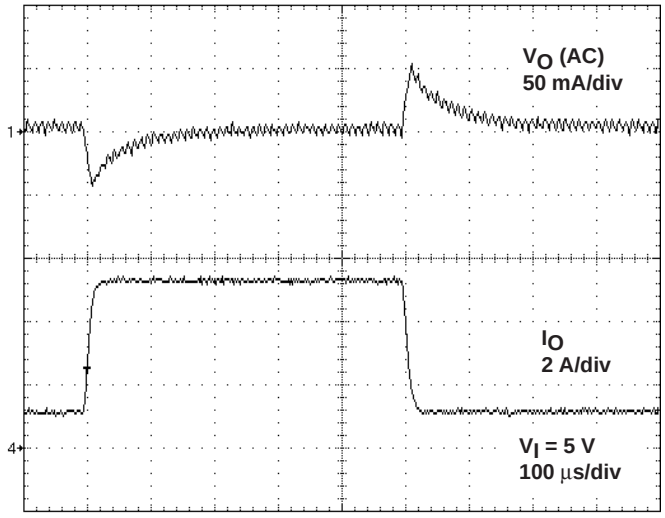
Figure 2–7. Measured Line Regulation



2.6 Load Transients

The TPS54610 EVM response to load transients is shown in Figure 2–8.The load transient in Figure 2–8 transitions from 1 A to 5 A in 10 µs. The output voltage deviates approximately 50 mV from its average value as a result of these transients.

Figure 2–8. Measured Load Transient Response



2.7 Loop Characteristics

The loop gain and phase for a 5.0-V input and a 6.0-A load are shown in Figure 2–9 and Figure 2–10. The loop crossover frequency is approximately 25 kHz, and the phase margin is approximately 75°.

Figure 2–9. Measured Loop Gain

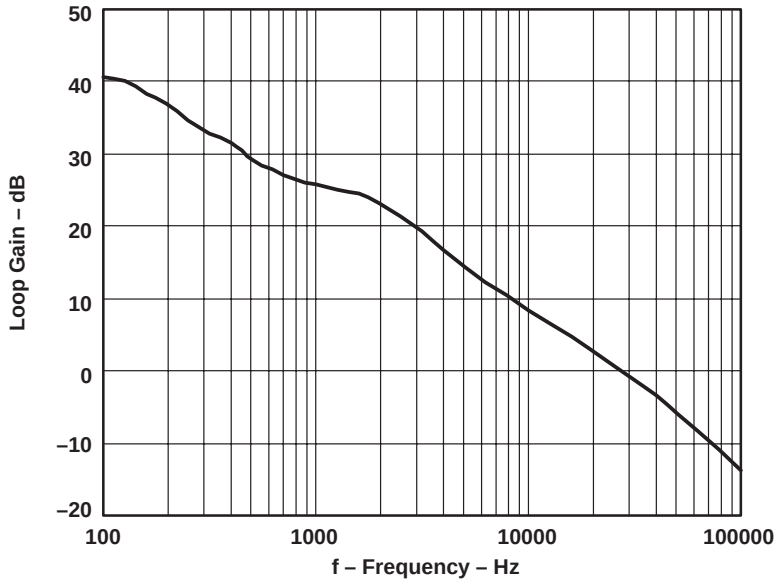
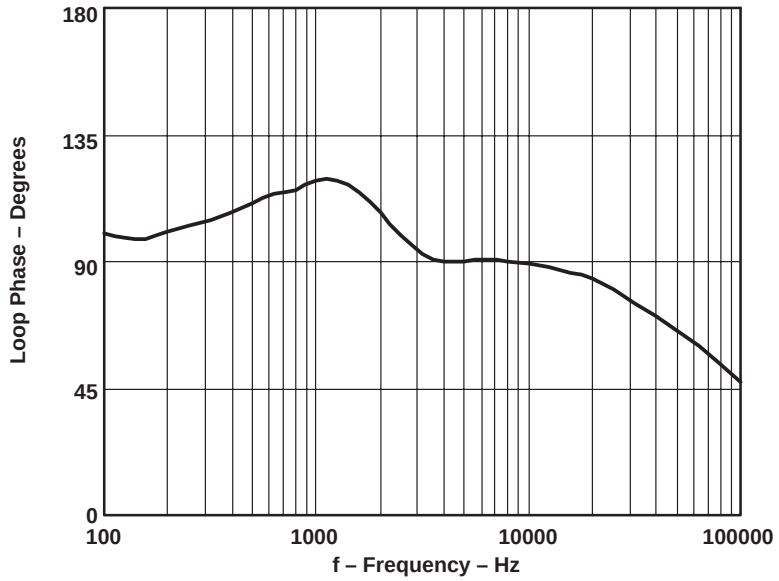


Figure 2–10. Measured Loop Phase



2.8 Output Voltage Ripple

The output ripple voltage is plotted in Figure 2–11 for a switching frequency of 350 kHz and in Figure 2–12 for a switching frequency of 550 kHz. The SLVP192 has a typical output voltage ripple of less than 18 mV_{pp}.

Figure 2–11. Measured Output Voltage Ripple at 350-kHz Operation

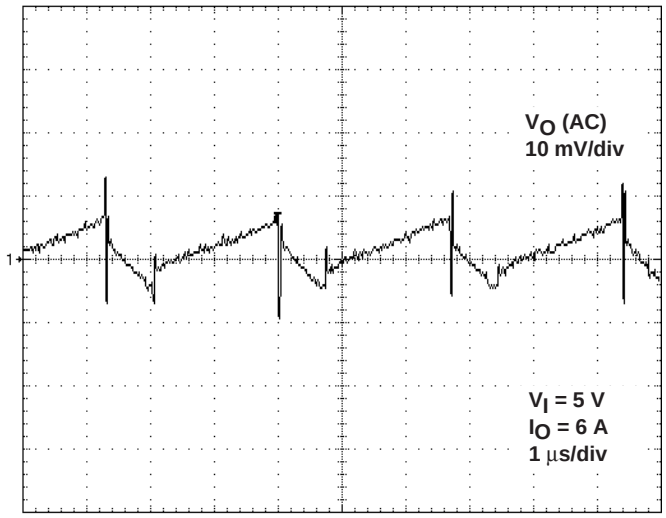
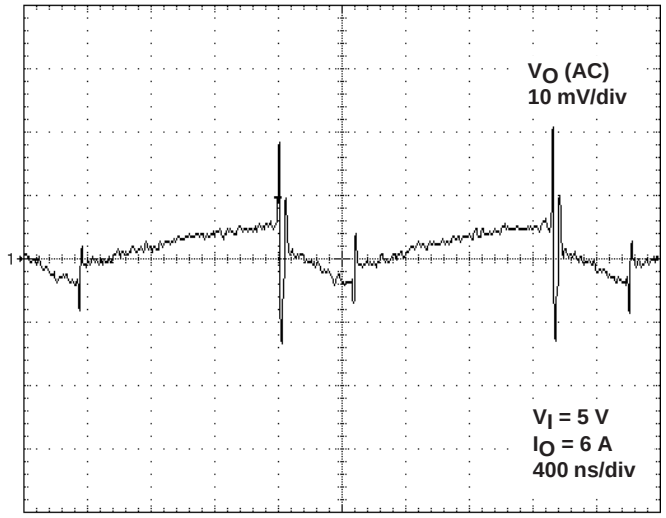


Figure 2–12. Measured Output Voltage Ripple at 550-kHz Operation



2.9 Input Ripple Voltage

The input ripple voltage for a 6-A load is shown in Figure 2–13 with a switching frequency of 350 kHz and in Figure 2–14 with a switching frequency of 550 kHz. With a switching frequency of 550 kHz, the input ripple is approximately 200 mV_{pp}. The input ripple voltage can be made lower by adding capacitance to the input.

Figure 2–13. Measured Input Voltage Ripple at 350-kHz Operation

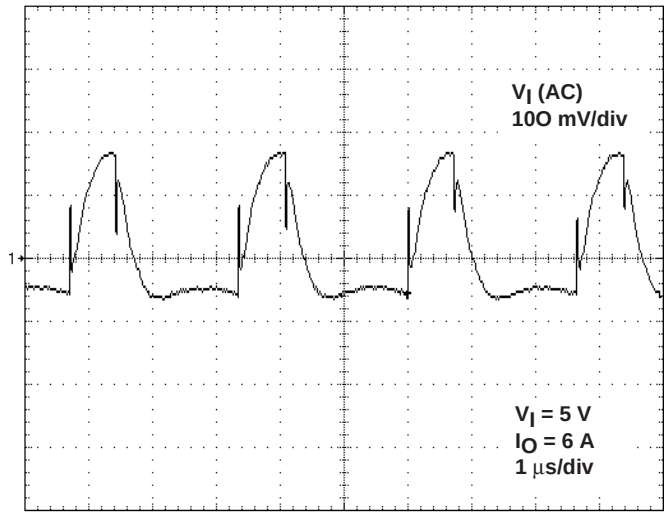
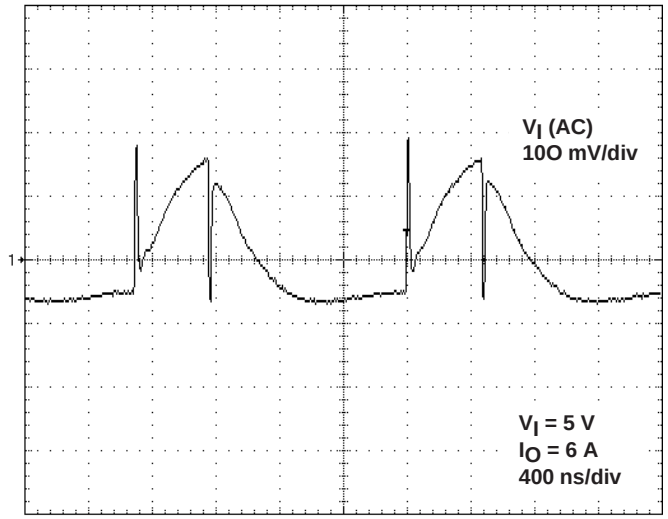


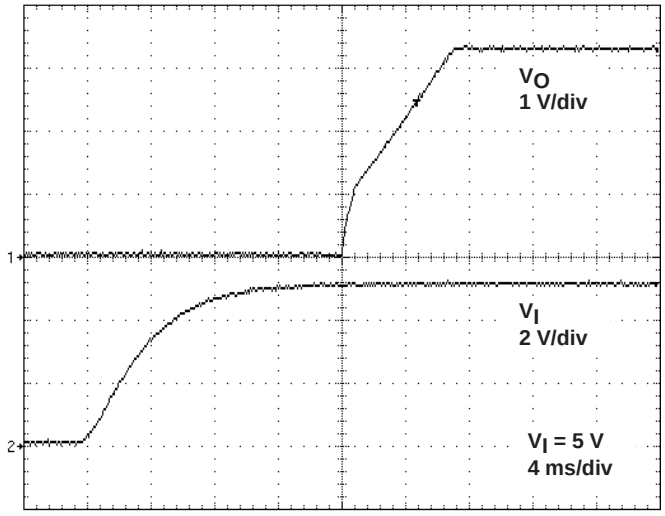
Figure 2–14. Measured Input Voltage Ripple at 550-kHz Operation



2.10 Start-up

The start-up voltage waveform of the TPS54610 EVM is shown in Figure 2–15. There is approximately a 12.8-ms delay after the input voltage rises above the 3.0-V start-up voltage threshold before the TPS54610 EVM output begins to rise. The output voltage then ramps to 3.3 V in 7.2 ms. The change of slope in the output voltage rising edge occurs at the point where control of the TPS54610 EVM internal reference voltage changes from the internally controlled slow start to the externally controlled slow start. Decreasing the value of C2 can decrease the start-up delay time and slow start time. To program a specific slow start time, see Chapter 1, Section 1.3, *Modifications*. If C2 is left unpopulated, the start-up delay time is eliminated, and the slow start time is typically 3.6 ms.

Figure 2–15. Measured Start-Up Waveforms



Chapter 3

Board Layout

This chapter provides a description of the TPS 54610 EVM board layout and layer illustrations.

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3.1 Layout

The top-side (component) layer for the TPS54610 EVM is shown in Figure 3–1. The input decoupling capacitor (C9), bias decoupling capacitor (C4), and bootstrap capacitor (C8) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation (TP4).

All layers are shown on the following pages and resemble a layer stack-up encountered in a typical application. The top and bottom layers are 1.5 oz. copper, while the two internal layers are 0.5 oz. copper. The two internal layers are identical and are used as *quiet* ground planes. The power ground plane is routed on the top layer, and is tied to the *quiet* (analog) ground planes at the output sense point (test point TP8). A wide power ground plane is used to keep the input ground current from injecting noise between the analog and power grounds. A total of 16 vias are used to tie the thermal land area under the TPS54610 device to the internal ground planes and to the thermal plane on the backside of the board.

Figure 3–1. Top-Side Assembly

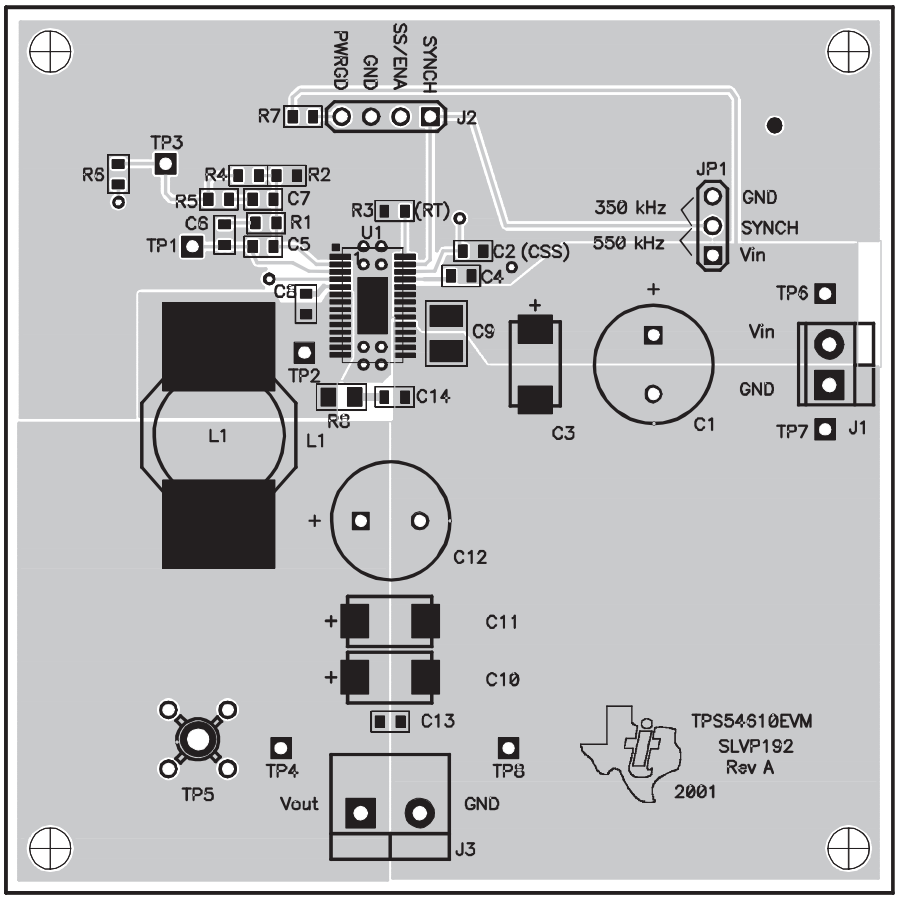


Figure 3–2. Top-Side Layout

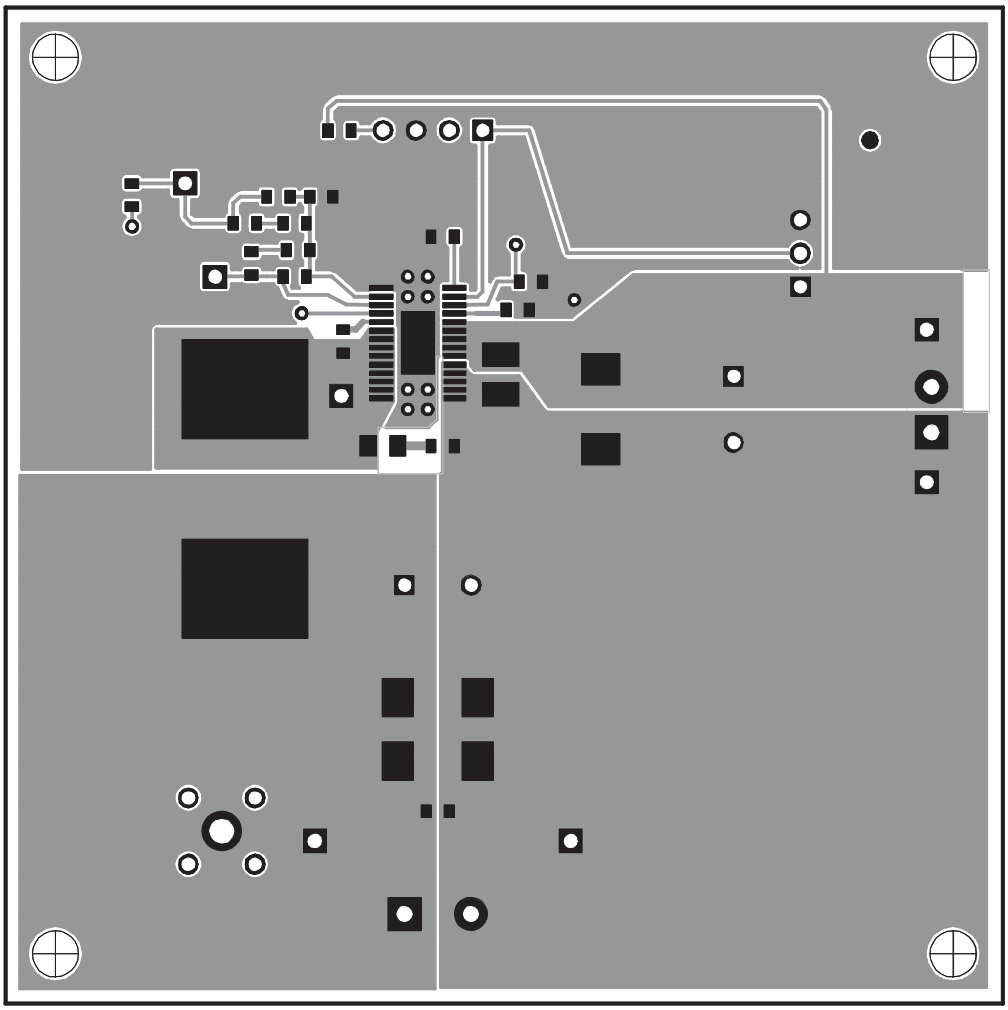


Figure 3–3. Internal Layers

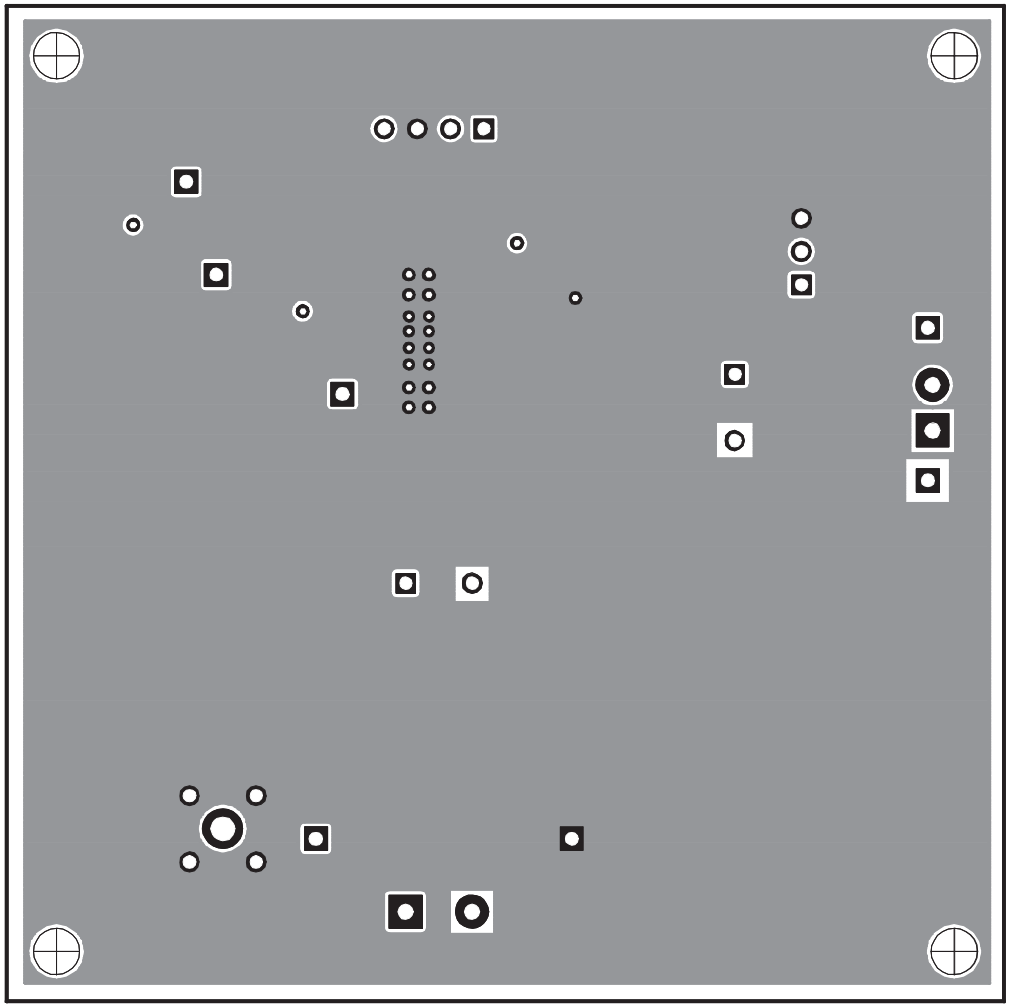
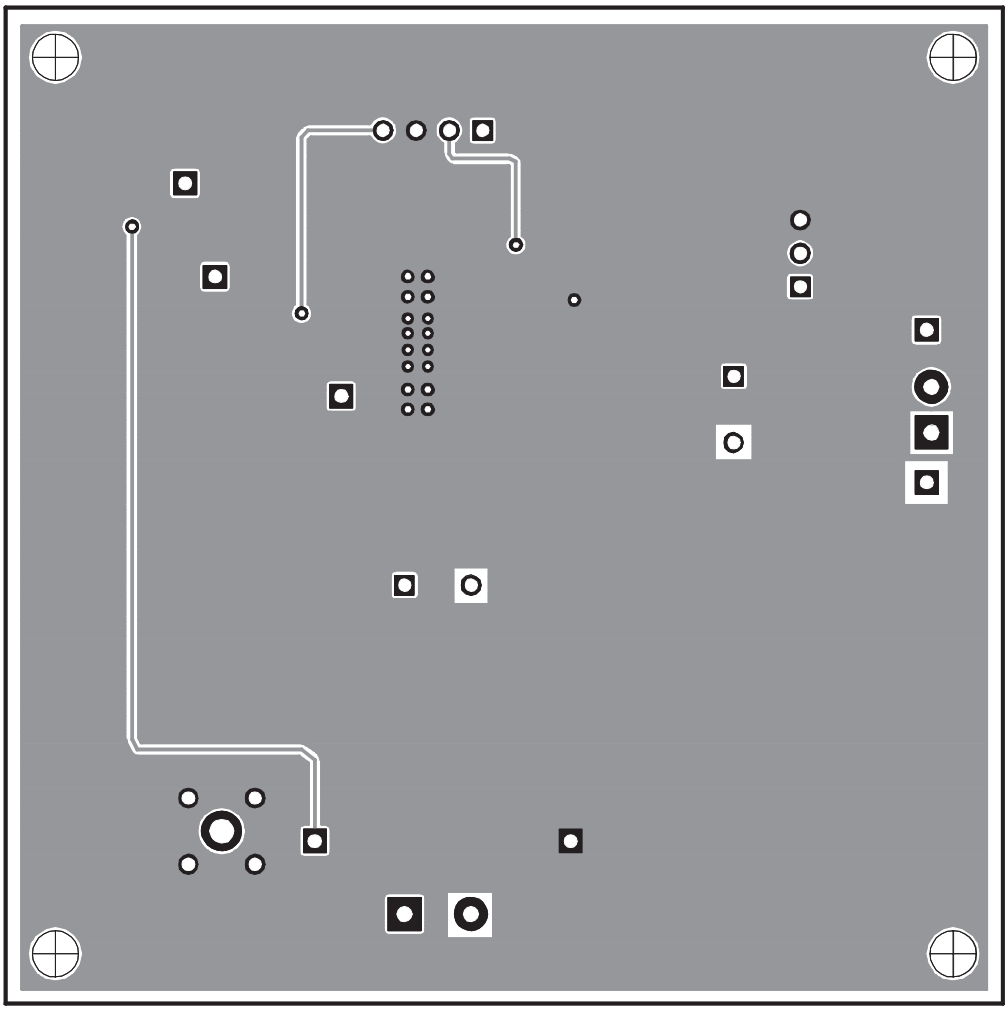


Figure 3–4. Bottom-Side Layer



Chapter 4

Schematic and Bill of Materials

The EVM schematic and bill of materials are presented in this chapter.

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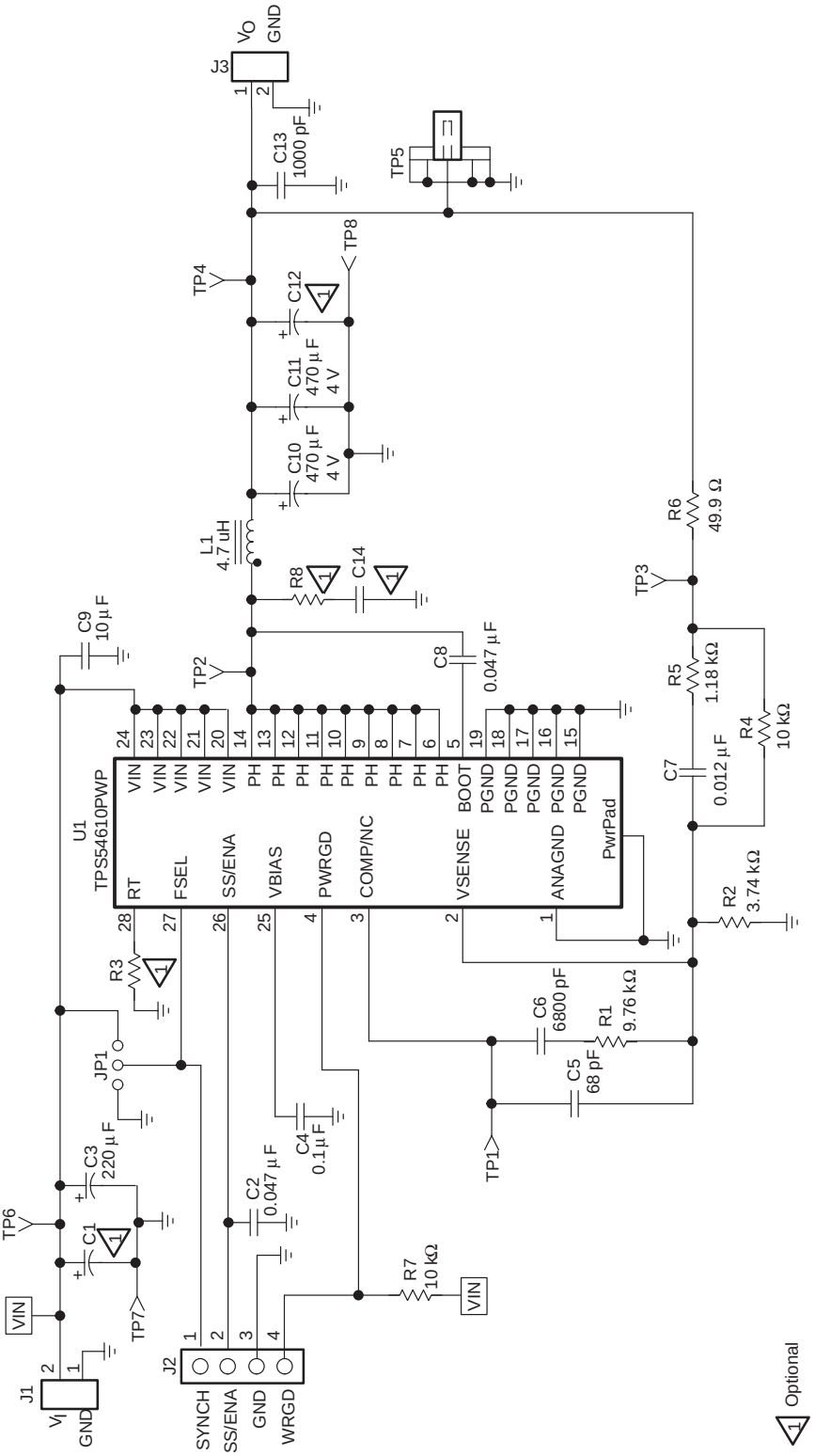
4.1 Schematic

Figure 4–1. TPS54610 EVM Schematic



4.2 Bill of Materials

Table 4–1. TPS54610 EVM Bill of Materials

Count	Ref Des	Description	Size	MFR	Part Number
—	C1, C12	Open	0.394		
2	C10, C11	Capacitor, POSCAP, 470 μF, 4 V, 40 mΩ, 20%	7343 (D)	Sanyo	4TPB470M
1	C13	Capacitor, ceramic, 1000 pF, 25 V, X7R, 10%	603	Murata	GRM39X7R102K25
	C14	Open	603		
2	C2, C8	Capacitor, ceramic, 0.047 μF, 25 V, X7R, 10%	603	Murata	GRM39X7R473K25
1	C3	Capacitor, POSCAP, 220 μF, 10 V, 40 mΩ, 20%	7343 (D)	Sanyo	10TPB220M
1	C4	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	603	Murata	GRM39X7R104K25
1	C5	Capacitor, ceramic, 68 pF, 50 V, C0G, 5%	603	Murata	GRM39C0G680J50
1	C6	Capacitor, ceramic, 6800 pF, 25 V, X7R, 10%	603	Murata	GRM39X7R682K25
1	C7	Capacitor, ceramic, 0.012 μF, 50 V, X7R, 10%	603	Murata	GRM39X7R123K50
1	C9	Capacitor, ceramic, 10 μF, 10 V, X5R, 20%	1210	Panasonic	ECJ-4YB1A106K
1	J1	Terminal block, 2 pin, 6 A, 3,5 mm	0.27 x 0.25	OST	ED1514
1	J2	Header, 4 pin, 100 mil spacing, (361–pin strip)	0.100 x 4	Sullins	PTC36SAAN
1	J3	Terminal block, 2 pin, 15 A, 5,1 mm	0.40 × 0.35	OST	ED1609
1	JP1	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 4.7 μH, 7.7 A, 12 mΩ	0.76 x 0.52	Coiltronics	UP3B-4R7
1	R1	Resistor, chip, 9.76 kΩ, 1/16 W, 1%	603	Std	Std
1	R2	Resistor, chip, 3.74 kΩ, 1/16 W, 0.1%	603	Std	Std
	R3	Open	603		
1	R4	Resistor, chip, 10 kΩ, 1/16 W, 0.1%	603	Std	Std
1	R5	Resistor, chip, 1.18 kΩ, 1/16 W, 1%	603	Std	Std
1	R6	Resistor, chip, 49.9 Ω, 1/16 W, 1%	603	Std	Std
1	R7	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Std
—	R8	Open	805		
5	TP1–TP4, TP6	Test point, red, 1 mm	0.038	Farnell	240-345
1	TP5	Adapter, 3.5-mm probe clip (or 131-5031-00)	0.2	Tektronix	131-4244-00
2	TP7, TP8	Test point, black, 1 mm	0.038	Farnell	240-333
1	U1	IC, SWIFT™ power controller, adjustable-V, 6 A	PWP28	TI	TPS54610PWP
1	—	PCB, 3 In × 3 In × 0.062 In		Any	SLVP192
2	—	Shunt, 100 mil, black	0.100	3M	929950-00